Integrated Photonic and Electronic Circuits Using CMOS Technology

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ABSTRACT

A massive growth is about to begin in the optical components sector, which will reorganize its business procedures and guarantee its financial success over the next three decades. Assembled circuits' processing capacity increased provides a cost-effective platform for the separation of electrical and photonic functions. Microsystems Technology Office is conducting a high-payoff R&D effort with the help of BAE Systems, Lucent Technologies, MIT, and Applied Wave Research. The program's ultimate objective is to provide the know-how and design instruments required to manufacture an electronic-photonic IC tailored to a particular use case (AS-EPIC). The construction of this demonstration platform includes investigating certain features often found in the front end of mixed signal receivers, such as detection, filtering, and modulation. Construction of the chip will take place at the Microphotonics Institute at MIT and the CMOS foundry at BAE Systems. We'll provide the most recent findings on the functionality of High Index Contrast Waveguides, Optical Filter Slices, and Modulators that are CMOS-Compatible. Based on the MIT Microphotonics Center Industry Consortium's newly released Communications Technologies Roadmap, we'll talk about the state of these developments.

Keywords: EPIC, Optical Filters, Waveguides, Modulators, Photodetectors

1. Introduction.

More and more, photonics must be integrated with electronics in order to keep the performance roadmap known as Moore's Law [1][2]. To date, the performance gains brought forth by parallelism have outpaced "Moore's Law's" prediction of a 2-fold increase in computing power every 18 months by a factor of ten. Photonic connectivity is simpler to construct than electronics with sophisticated compensating circuits due to the virtual threshold imposed by data speeds of 10Gb/s per channel for connections of >1m. Beyond connectivity, coupled electronic-photonic signal processing is starting to become useful in fields like Rapid Fourier Transforms. These considerations suggest that as design expertise grows, the future will see less of an electronics-to-photonics replacement and more of a segmentation of function. In the near future, a CMOS chip manufacturing process will be required that can integrate electrical and unimpeded transmission of photonic signals, devices, and functional circuits [4][5].

Recent publications from the MIT Communications Technology Roadmap provide an assessment of the several novel photonic technologies that have shaken up the telecoms sector. There were four main takeaways from the report:

- There is no one place to go to get the skills necessary for this road.
- There will be a dramatic leadership change in the underlying component business from telecom to IT as a result of this move (computing, imaging).

• Short-range connectivity (less than 1 kilometer) will be prioritized for functional purposes.

• Electronic-photonic convergence is the key to understanding the components technology of the future.

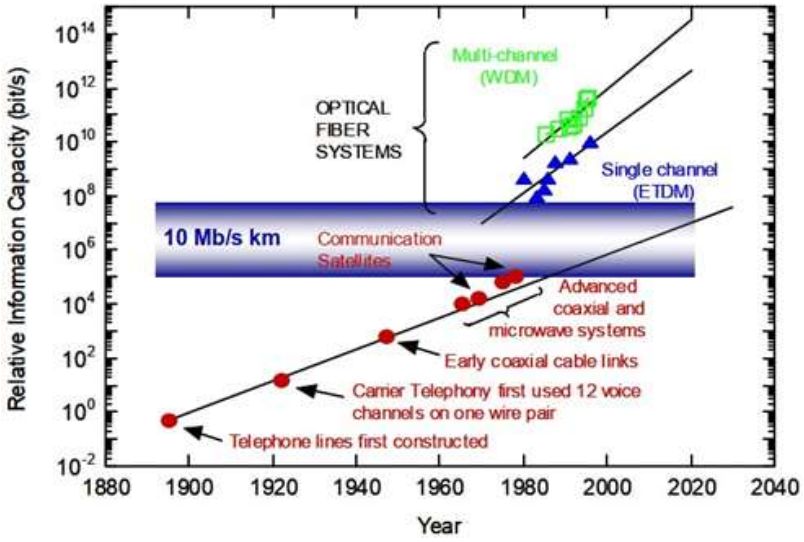

Fig. 1. Graphing the equivalent data rate of a single line across time, colored by the year in which a certain technology was introduced, provides a timeline view of the development of information transport technology. With optical transfer, the slope and rate of performance improvement become more abrupt [5][6].

In the next decade, the roadmap aims to implement four key features: The construction of One estimate puts the potential annual revenue at $20 billion, It is expected that technological obsolescence will drive the sector ultimately via increased performance. scaling, with product lives substantially shorter than the telecoms network development cycle [7][8].

There are two main uses for Electronic Photonic Integrated Circuits (EPICs): connectivity and signal processing. Five years ago, connectivity was thought to be the sole use for photonics. Increased processing performance may now be had with much reduced power consumption, footprint, and weight; this is especially true for applications in sophisticated signal processing like channelization. Our initial steps toward implementing EPIC OSP built on BAE Systems' CMOS technology are summarized below, along with the lessons we've learned and the progress we've made so far [9][10].

2. Incredible CMOS System Platform

One of the first monolithic electronic-photonic integration on the silicon wafer platform, our AS-EPIC chip is used in signal processing. Input RF signals may have their Fourier transforms performed quickly and accurately using this device. An electro-optic modulator encodes the radio frequency signal onto an optical carrier; an optical filter network channels the signal into discrete frequency bands; and a specialized photodetector decodes the signal from each channel. Integrated Instead of the size, power consumption, noise of the individual devices and bandwidth, the critical performance metrics are the What the E-P circuit does [11][12]. A circuit may be used in a complementary metal oxide semiconductor enhanced field-effect transistor of many standard-issue devices to accomplish the same, albeit more complex, signal-processing task than the 3R (relock , reshape ,reamplify) signal conditioning used in long-haul telecommunications, which relies on individually optimized discrete-device performance at each node. Typical microwave signal processors have been slimmed down in size, weight, and power consumption in order to channelizing application makes use of a new class of "technology shrink" features that encode on an optical carrier. Ring resonators are only one example of a device that has a microwave counterpart. Our research shows

that many of the same principles employed in microwave circuit design also apply to to EPIC.

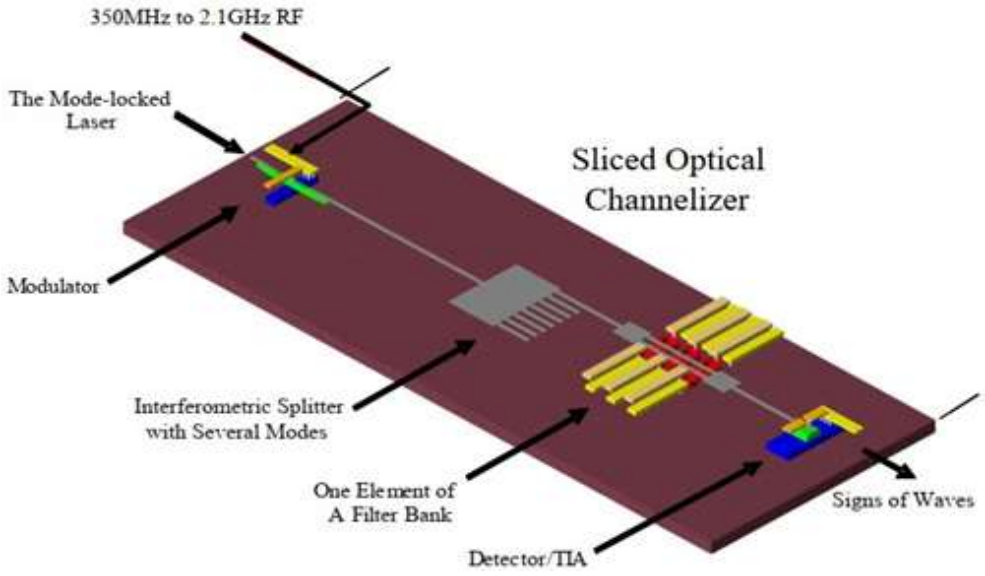

Fig. 2. A simplified diagram of the AS-EPIC chip's lone channelizer connection.

In Figure 2 we can see a diagram of the components that make up our circuit. The modulator/driver is the initial component of E-P integration, since it is responsible for encoding the RF signal into the optical carrier. The carrier is connected to the device via an external mode-locked laser, making use of an "optical power supply" design. It is always the case that the optical carrier frequency is much greater than the RF signal frequency. The efficiency of the source and the architecture of the modulator and waveguide will determine the optimal wavelength. High-performance light sources nowadays are optimized for long-distance communications and typically operate at 1570 nm, the wavelength at which fiber transparency is highest. As a result, E-P circuits that function at these wavelengths are advantageous [13][14].

Compatibility with CMOS technology should not be a limiting factor in materials selection. After the optical source limitation is eliminated, materials like Si, SiO2, Si3N4, Ge, and related alloys work well for our designs and best fulfill the integration requirement. In order to achieve ultra-dense integration, micron-turn radii are required, and silicon's large index contrast with a SiO2 cladding (nSi/nSiO23.5/1.5) makes this possible. As silicon has a high refractive index, it is easy to match impedances for waveguide coupling to active modulator (n=4.2) and photodetector (n=5.1) devices. At this point in time, germanium is used for photodetectors whereas silicon is used for waveguides, modulators, and filters. Even if these devices' performance is up to par, some additional work may be required to optimize the materials used so that they may be more easily integrated into production.

Ring resonator structures are used to do frequency-domain filtering of the optical signal. An analogous Fourier Transform of the input RF signal is provided by an array of filters, each of which is set to a different RF frequency channel. The optical signal is converted to an electrical regime for A/D conversion at the subsequent E-P node, the photodetector/TIA, after channelization. We need to hit a number of targets in order for our AS-EPIC chip's circuit to function well. In order for the circuit to function properly, the SFDR requirements need a very linear signal path from the modulator/driver to the detector/TIA. Narrow band filters and low power dissipation both need optical waveguides with minimal loss. To achieve the needed high digital resolution, powerful photodetector/TIA nodes are essential. The primary goals of the first EPIC development program are to design, prototype, and qualify device modules for each node in the circuit, demonstrating the

manufacturing cycle for monolithic integration in the BAE Systems CMOS foundry. This study explores these problems and how they are affected by materials, processes, and process integration [16].

3. Device performance the EPIC

3.1. Fiber optic waveguide

Dense E-P integration places limitations on waveguide design in terms of Aspect ratio (height /width), number of vertical layers, transmission loss (dB/cm), and radius of curvature (m). The complementary metal-oxide semiconductor (CMOS) technology employs both deposited upper-level waveguides wafer-level and. Because of the significant index difference between Si and SiO_2, this material system must be used as a waveguide for efficient E-P integration. Wafer-level signal transmission was investigated using single crystal silicon-on-insulator (SOI), whereas higher-level waveguides were investigated using chemical vapor deposited (CVD) silicon. silicon impurity/defect absorption, sidewall roughness scattering, substrate/surrounding feature radiation are the key factors of transmission loss. After receiving these smoothing treatments, SOI showed no signs of material loss and functioned well. The material loss of deposited silicon might be controlled by adjusting the deposition conditions. Vertical and lateral layout exclusion design guidelines were created to reduce radiative loss. We have summarized the loss performance under normal processing settings in Table 3.1.

Table 3.1.
Silicon waveguides designed in 0.16 μm technology and produced in the BAE CMOS line: design and performance.

Waveguid Type	Thickness the Layer	Size of the Cladding	Loss
Deposited Si	210 nm	2 μm	3 dB/cm
SOI	210 nm	2 μm	0.30 dB/cm

Based on the guidelines for process integration, two different smoothing procedures were adopted. Global sidewall roughness was reduced using dry oxidation smoothing (vapor phase). Most effectively, oxidation and stripping were carried out in tandem. In situations. The best loss performance was achieved with the most refined versions of this procedure. Generally, a loss of less than 0.4 dB/cm is preferred for very long signal routes. For higher-level, shorter signal pathways, we use deposited waveguides with 3dB/cm and SOI waveguides with 0.30dB/cm employing a 2μm oxide standoff from the substrate [20][21].

There is a relationship between bend loss and the turn radius, the processing of the sidewalls, and the waveguide layout. We have shown minimal loss signal transmission across 2 μm radius bends, and for 11 μm and larger, there is no quantifiable loss in our most permissive designs. In order to quantify the loss, two techniques were used the cutback loss was measured using a JDS Uniphase Swept Wavelength System, while the ring resonator loss was measured with a LUNA Optical Vector Analyzer.

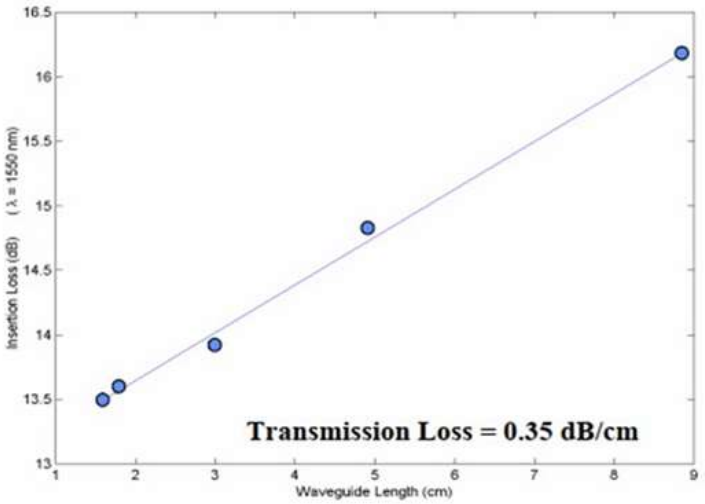

Fig. 3. An SOI waveguide coated in SiO_2 and made on the BAE CMOS line has its cutback loss measured.

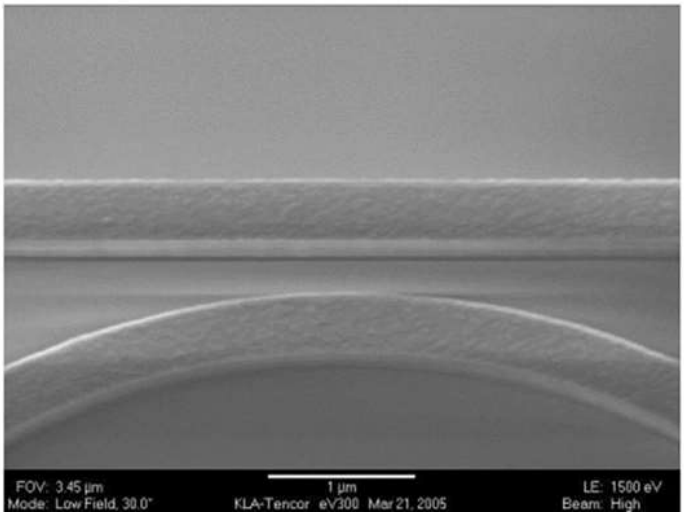

Fig. 4. This scanning electron micrograph (SEM) shows a 0.18 µm CMOS manufactured silicon waveguide and ring resonator. The clad waveguide has a transmission loss of 4 dB/cm.

3.2. The Optical modulator

An all-silicon modulator with high throughput, low power consumption, and simple integration has been created. This ring resonator layout has a modest physical profile as an added bonus. The gadget works by changing the index of refraction of silicon using free carriers.

Carrier injection via two-photon absorption was used to prove the device worked; in this case, the reaction time was established by the minority carrier lifetime. When an extra carrier sweep-out voltage is applied, the device's processing speed increases dramatically. Our apparatus uses a lateral p-i-n junction to accomplish sweep-out and the functions of carrier injection. The size of the device, the needed power dissipation and sweep-out current, they are all drastically decreased by the resonator construction.

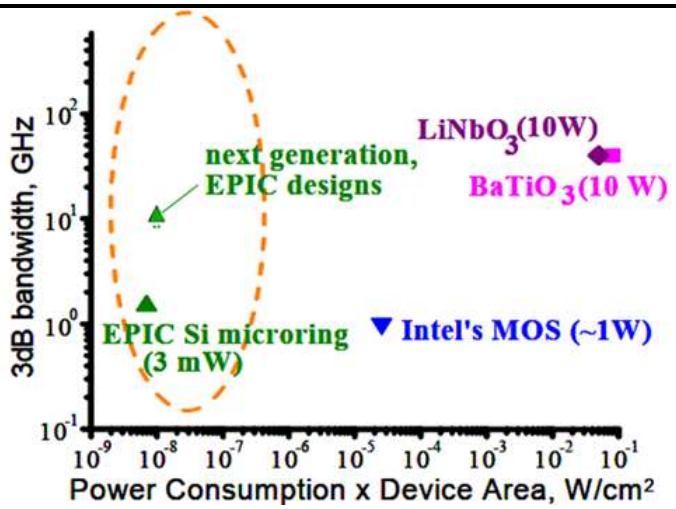

Fig. 5. Analyzing the Si ring modulator's performance in relation to those of other common modulator types. Monolithically integrated EPIC devices have a performance goal indicated by the dashed region.

A modulator performance design diagram is shown in Figure 5. Maximum modulation frequency, modulation size, on-off transition rate, insertion loss, operational voltage, and power supply voltage are all important design limitations (equivalent V for full modulation depth). An integrated active device's inverse square speed is one of its advantages (power x footprint). Figure 5 shows that $LiNbO_3$ and $BaTiO_3$ discrete devices' high speed comes with a high (power x footprint). Similar free carrier index adjustment is used in Intel's integrated MOS modulator, however this nonresonant device has high power and size requirements. Using mW powers.

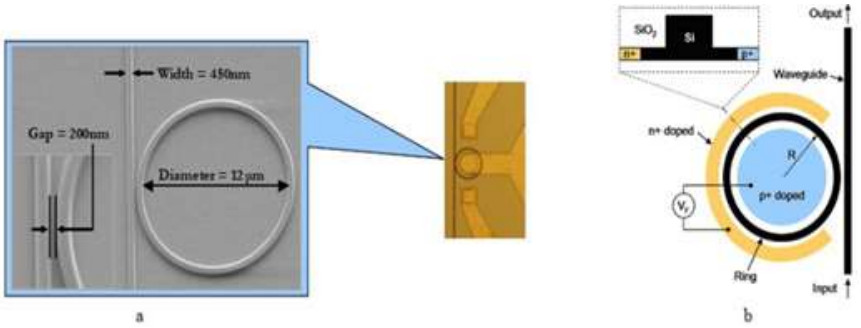

Fig. 6. Two views of the Si ring modulator are shown here

The device is seen in planar and cross-sectional perspectives in Figure 6. The results of some of the measurements are shown in Figures 7a and 7b. The variation of the silicon ring's resonant frequency in response to an injected current is seen in Figure 7a. Return-to-zero (RZ) performance of 1.4Gb/s is shown by the temporal dependency of the voltage drive and optical modulation, as shown in Figure 7b. When compared to other reported modulators, this one offers the lowest power usage and smallest footprint. Full 10dB modulation depth may be achieved with a dc supply of less than 0.35V and 1mA. It takes 3.2V and 1mA under ac circumstances. This efficiency is well within our ASEPIC circuit's modulator's 9.5mW power allowance. As an analog signal processing function, our channelization circuit's device linearity and other properties are crucial. The preliminary findings in the inset of Figure 7a suggest that this device construction has high potential for a linear response.

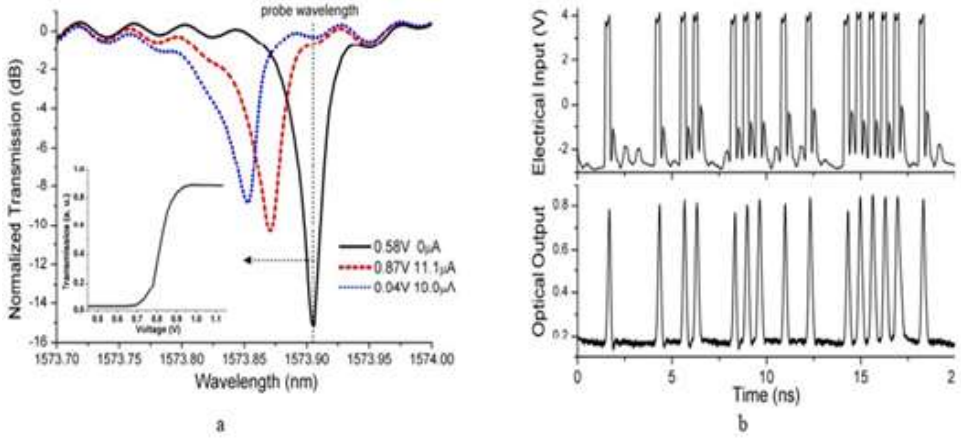

Fig.7. (a) the effect of the injection on the ring

3.3. Filtering light using an optical system

Our circuit relies on an optical filter to provide highly selective frequency bands. The high-Q ring resonator architecture and the Mach-Zehnder filter arrangement allow for precise channeling. Dimensions, center frequency, insertion loss, and channel shape (1.7dB and 27dB channel widths) are the performance requirements. In order to be useful for Wavelength Division Multiplexing, these ultra-high-resolution filters need to have channel widths of just 1.3 GHz, down from 99 GHz. Channel specifications and waveguide loss-induced deterioration of channel shape are shown in Figures 8a and 8b, respectively. The pass-band is widened and rounded out, while the stop-band is narrowed, and the insertion loss increases dramatically.

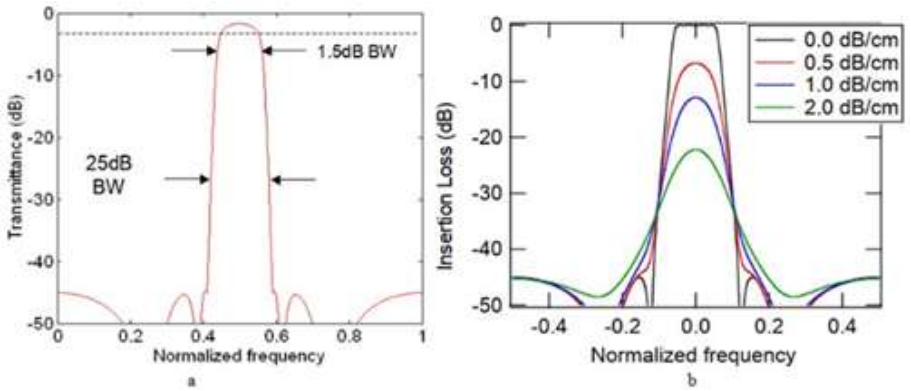

Fig. 8. Channel form requirements in optical filter design (a) and the impact of waveguide loss on channel profile (b).

Notwithstanding the great accuracy that CMOS pattern transfer may reach, it is very unlikely that uniformity on a wafer level can be attained throughout the design and process development phases. Moreover, unlike discrete devices, performance cannot be "binned" for integrated filter arrays. For optimal performance, a design that is both fault-tolerant and resilient must allow for trimming and adjusting. We have shown that a polysilane clad layer can be tuned to a certain frequency by exposing it to a controlled amount of UV light. Several versions of filter designs have been manufactured at the CMOS foundry at BAE Systems for this program. Using the CMOS platform's multilayer, back-end metallization for heater placement, we discover that precise thermo-optic adjustment is possible. We have also shown that these circuits are capable of lossless thermo-optic switching. The results of these efforts will be disclosed in the near future. In conclusion, our process runs at BAE Systems' Optical filter performance may be maximized and new densities of E-P integration can be achieved, according to research conducted by CMOS foundries.

3.4. Photodetector

When it comes to integrating photodetectors with CMOS circuits, germanium is the material of choice. Since its bandgap is narrower than silicon's, it is absorbent to light wavelengths that flow without loss in silicon waveguides, and it is compatible with silicon, providing a full solid solution. Also, germanium is an excellent choice for detectors. The 1540 nm telecommunications standard is surrounded by a band structure consisting of a highly absorbing direct gap. wavelength, and the carrier mobilities are about four times larger than in silicon. Since real CMOS integration no longer needs massive graded buffers, it has recently been possible to create essentially dislocation-free Ge-on-Si. In Figure 9, we see a performance design diagram for a Ge photodetector. The product of the detector's bandwidth and quantum efficiency has traditionally been used as a conventional FOM for performance. The footprint measure is added for E-P integration. The advantages of integrating a waveguide detector are that the photon flow is perfectly focused, and the detector's impedance is perfectly matched to the source. There are two major advantages. The first benefit is that the detector may be made as tiny as the cross section of the waveguide. Widths of 0.5-1 μm are common for 1540 nm single mode silicon waveguides. Until device RC time constants start to restrict speed, detector lengths of >100 μm are feasible. Second, very short transit distance p-i-n detectors are suitable for designing the waveguide-detector connection.

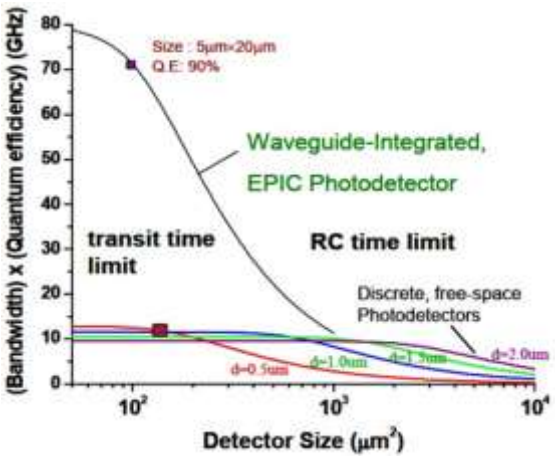

Fig. 9. Schematic depicting the layout for a Ge-on-Si photodetector. EPIC detectors will have improved quantum efficiency, quicker readout times, and smaller footprints.

Figure 10 provides a clear illustration of the advantages of these features. Operation wavelength, responsiveness, compactness, speed, and efficient waveguide coupling are some of the design requirements for integrated photodetectors.

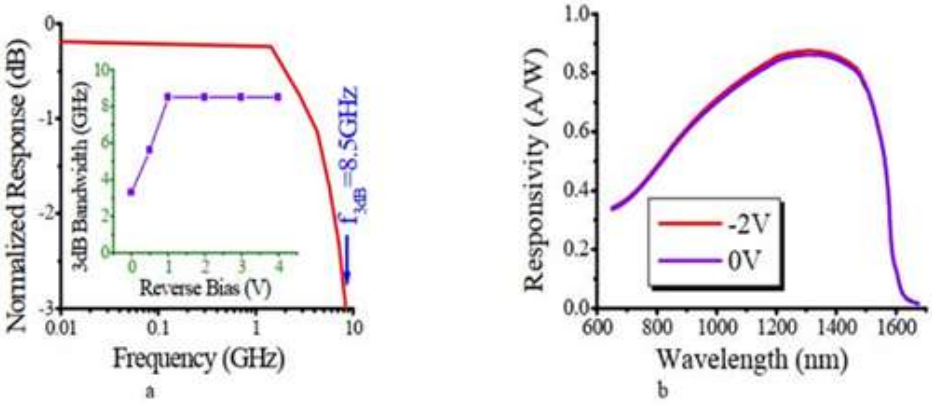

Fig. 10. (a) frequency response of a Ge-on-Si photodetector, with an inset demonstrating 1V operation; (b) a responsivity spectrum demonstrating almost perfect behavior during biased and unbiased operation.

Strain engineering has allowed us to enhance the detection range of our previously proven Ge photodetectors from 650 to 1600 nm. Over 650-1345 nm, the overall internal quantum efficiency is more than 92%. The bandwidth of the detector was found to be 8.8GHz at 980nm and 2.8GHz at 1540nm. Because the transit zone is so narrow, it operates perfectly well at VR<1V. The measured response time and frequency spectrum are shown in Figures 10a and 10b. The 'bufferless' Ge-on-Si deposition method is crucial to CMOS integration. Two-step UHV-CVD growth and a post-depositiondefect elimination anneal are the major components of the method. Currently, no other kind of Ge photodetector can match the performance of these Ge-on-Si detectors.

We have developed and tested waveguide-coupled detector designs at MIT to establish EPIC program guidelines for detector construction. In Figure 11, we can see the results of using silicon detectors with SiON waveguides, where the refractive index was adjusted by varying the amount of nitrogen in the waveguide. Our models were validated by the data, which showed that a smaller index difference between the waveguide and detector resulted in a longer coupling length and higher coupling efficiency for evanescent coupling. We have shown that with an index difference of 2, a detector 100 μm in length may achieve an efficiency of 85% in coupling. The EPIC circuit's lower index difference (nSi - nGe = 0.5) is predicted to have a coupling efficiency close to 100% for a length of coupling significantly less than 50 μm.

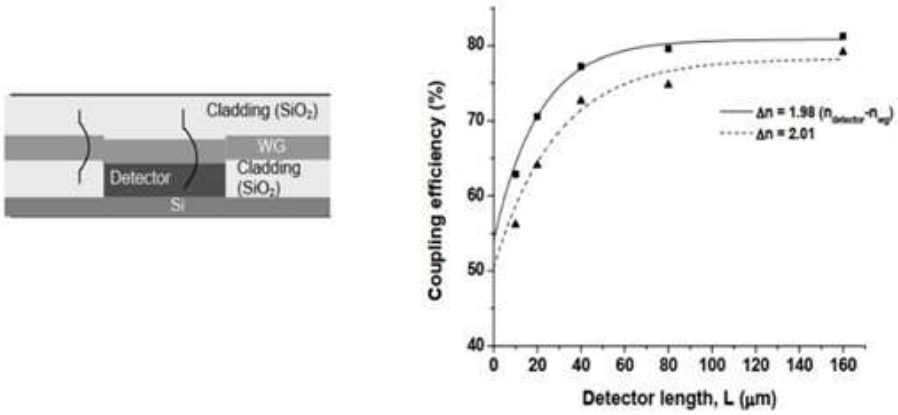

Fig. 11. This article describes the design and operation of a detector that uses two waveguides that have a distinct index of refraction. There is a 1.98 point discrepancy between the detector and waveguide in the solid graph and a 2.01 point difference in the dashed graph. In terms of coupling speed and efficiency, the higher index waveguide (lower Δn) is clearly superior than the lower n waveguide.

3.5. Integration of E-P circuits

Integrating electrical and photonic circuits at a high level of performance requires the resolution of many critical difficulties. The biases of the detectors must be within the specification for the CMOS supply voltage being used. Large current swings need to be handled by the modulator driving circuit. Photonic circuits must be protected against thermo-optic imbalance brought on by heat generated by high-speed electronic circuitry. There has to be dielectric separation between the optical signal and any nearby electronics. The connection between the signal processors used in channelization must remain linear. Strong first-order designs have been created and show the way to peak efficiency.

4. Integration of CMOS Processes

For our highly integrated optical signal processor chip, we have established a set of design guidelines. Photonic device count, electronic device count, size, and power dissipation are the metrics. Constraints are imposed further by process integration. In Figure 12a, we can see a simplified cross-section of a CMOS chip, which comprises of a "front end" of FET devices on the wafer level and a "back end" of multilayer interconnections. To obtain the best density and performance in a process-compatible architecture, we define E-P CMOS integration as the optimal arrangement of electrical and photonic components at all layers.

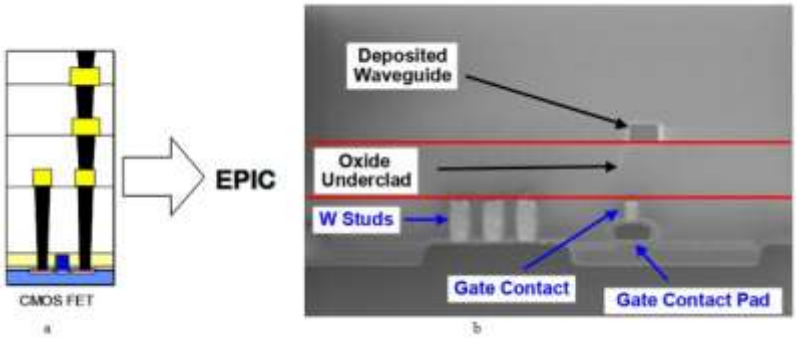

Fig. 12. EPIC chip cross section with waveguides, transistors, contacts, and connections

As was previously indicated, we observed that the precision thermo-optic tuning of our optical filter circuit benefited greatly from the accuracy of 0.18 μm CMOS architecture. We made choices between several possibilities until we arrived at the final 3-dimensional arrangement. Figure 12b shows a SEM slice through such a design. The location of junctions and dielectrics for electrical isolation mustretain integrated processing of active and passive photonic devices without compromising the electrical circuits' performance. It is crucial to optically isolate the Ge from the substrate while still preserving the epitaxial template for Ge development. Variations in layer depth and lateral spacing are required to create adequate isolation between floors. Plugs and vias must be constructed with practical aspect ratios to provide continued electrical access at all levels. There is use of both evanescent and butt optical coupling in the horizontal and vertical directions. Just Si, SiO_2, Si_3N_4, Ge, and SiGe are available to us at this time. At the Si-rich end of the SiGe alloy composition, CMOS now uses Ge, while our device is entirely at the Ge-rich end. In our level-by-level CMOS processing, the thermal budget sequence requires lower process temperatures at higher levels and, if feasible, the incorporation of heat treatments into the processes themselves to reduce the likelihood of thermal excursions. As E-P integration isn't just an extension of CMOS pattern transfer, practically every process qualification requires a solution to a contamination problem.

Conclusion

Initial designs and process implementations for an ap-epic electronic photonic integrated circuit have been created at the BAE Systems CMOS foundry (AS-EPIC). For radio frequency signals, our technology will offer a channelization function similar to a Fast Fourier Transform within its operating frequency range. A waveguide, optical modulator, optical time domain filter, couplers, and photodetectors were built for CMOS implementation as part of an optical signal processor link, along with device design guidelines and process integration design rules. Thus far, testing has shown that the devices and circuits perform at state-of-the-art levels. For single crystal silicon on insulator (SOI) waveguides, the transmission loss is 0.35dB/cm, whereas for CVD-deposited polycrystalline structures it is 4dB/cm. That's the optical filter is precisely tuned using thermo-optics, and it may be switched between modes without incurring any signal loss. With a diameter of 10-12 μm and an ac power dissipation of 3 mW, the silicon ring-resonator modulator boasts a digital performance of 1.5

Gb/s and an extinction ratio of 15 dB. The germanium photodetector can detect light with a wavelength of 1500nm and a bandwidth of 2.5GHz at a bias of <1V. Its responsivity is >0.8A/W.

When it comes to E-P integration and overall performance, the EPIC program is unparalleled. With the program's sustained success, microwave signal processing might see a reduction in size, weight, power consumption, and cost while also being able to function at a better level.

The same holds true for this technology's commercial release, which might be brought up by up to 10 years. There is reason to be optimistic about our ability to demonstrate the full EPIC capability envisioned by DARPA MTO, given our substantial progress in this direction and the promise of future integration with already demonstrated, CMOS-compatible modulator and detector building blocks, such as low loss silicon waveguides and adaptive optical filters fabricated on the BAE Systems CMOS production line.

References

1. Hassan, M. D., Nasret, A. N., Baker, M. R., & Mahmood, Z. S. (2021). Enhancement automatic speech recognition by deep neural networks. Periodicals of Engineering and Natural Sciences, 9(4), 921-927.
2. Mahmood, Z. S., Coran, A. N. N., & Aewayd, A. Y. (2019, October). The impact of relay node deployment in vehicle ad hoc network: Reachability enhancement approach. In 2019 Global Conference for Advancement in Technology (GCAT) (pp. 1-3). IEEE.
3. Mahmood, Z., Nasret, A., & Awed, A. (2019, September). Design of new multiband slot antennas for wi-fi devices. In International Journal on Communications Antenna and Propagation (IRECAP) (Vol. 9, No. 5).
4. Mahmood, Z. S., Nasret, A. N., & Mahmood, O. T. (2021, October). Separately excited DC motor speed using ANN neural network. In AIP Conference Proceedings (Vol. 2404, No. 1, p. 080012). AIP Publishing LLC.
5. Mahmood, Z. S., Coran, A. N. N., esam Kamal, A., & Noori, A. B. (2021, August). Dynamic spectrum sharing is the best way to modify spectrum resources. In 2021 Asian Conference on Innovation in Technology (ASIANCON) (pp. 1-5).
6. Nasret, A., & Mahmood, Z. (2019). Optimization and integration of rfid navigation system by using different location algorithms. International Review of Electrical Engineering (IREE), 14(4).
7. Mahmood, Z. S., Coran, A. N. N., & Kamal, A. E. (2018). Dynamic approach for spectrum sharing in cognitive radio. International Journal of Engineering & Technology, 7(4), 5408-5411.
8. Nasret, A. N., Noori, A. B., Mohammed, A. A., & Mahmood, Z. S. (2021). Design of automatic speech recognition in noisy environments enhancement and modification. Periodicals of Engineering and Natural Sciences, 10(1), 71-77.
9. NASRET, A. N., KAMAL, A. E., & MAHMOOD, Z. S. Radar Target Detection by Using Levenberg-Marquardt Algorithm.
10. Mahmood, Z. S., Kadhim, I. B., & Nasret, A. N. (2021). Design of rotary inverted pendulum swinging-up and stabilizing. Periodicals of Engineering and Natural Sciences, 9(4), 913-920.
11. Coran, A. N. N., Mahmood, Z. S., & Kamal, A. E. (2021, October). Classification of Acoustic Data Using the FF Neural Network and Random Forest Method. In 2021 International Conference on Smart Generation Computing, Communication and Networking (SMART GENCON) (pp. 1-4). IEEE.
12. Coran, A. N. N., Sever, P. D. H., & Amin, D. M. A. M. (2019). Acoustic data classification using random forest algorithm and feed forward neural network. In IEEE global conference for advancement in technology.
13. Laylani, L. A. A. S. S., Coran, A. N. N., & Mahmood, Z. S. (2022, January).

Foretelling Diabetic Disease Using a Machine Learning Algorithms. In 2022 International Conference for Advancement in Technology (ICONAT) (pp. 1-5). IEEE.

14. Kamal, A. E., Salih, A. B., & Coran, A. N. N. (2018). Spectrum sensing algorithm using ANN in cognitive radio. International Journal of Engineering & Technology, 7(4), 5151-5155.
15. Kadhim, I. B., Khaleel, M. F., Mahmood, Z. S., & Coran, A. N. N. (2022, August). Reinforcement Learning for Speech Recognition using Recurrent Neural Networks. In 2022 2nd Asian Conference on Innovation in Technology (ASIANCON) (pp. 1-5). IEEE.
16. Kadhim, I. B., Nasret, A. N., & Mahmood, Z. S. (2022). Enhancement and modification of automatic speaker verification by utilizing hidden Markov model. Indonesian Journal of Electrical Engineering and Computer Science, 27(3), 1397-1403.
17. Coran, A. N. N., Ali, A. H. M., Mahhmood, Z. S., & Mohammed, S. F. (2021, December). Design Speech Recognition Systems in the nosily Environment by Utilizing intelligent Devices. In 2021 Second International Conference on Smart Technologies in Computing, Electrical and Electronics (ICSTCEE) (pp. 1-6). IEEE.
18. Coran, A. N. N., Mahmood, Z. S., & Salih, A. B. (2018). Satellite network underlying LMS for coverage and performance enhancement. International Journal of Engineering & Technology, 7(4), 5404-5407.
19. Mezaal, Y. S., & Nasret, A. N. A New Microstrip Bandpass Filter Design Based on Slotted Patch Resonator.
20. Mahmood, Z. S. (2012). YÜKSEK LISANS TEZI.
21. Aaref, A., & Mahmood, Z. (2021). Optimization the accuracy of ffnn based speaker recognition system using pso algorithm. International Journal on Communications Antenna and Propagation (IRECAP), 11(4).